AMD Zynq UltraScale+ RFSoC P047_P047Pro User Manual

SDR & FPGA Solution Provider

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Version Records:

Date	Version	Description
2025.11.25	V1.0	initial version

This tutorial will be continuously revised, optimized, and expanded based on practical experience. Our goal is to provide you with more and better demos to aid your development as a field expert.

If you find any errors or have suggestions, please contact us.

Content

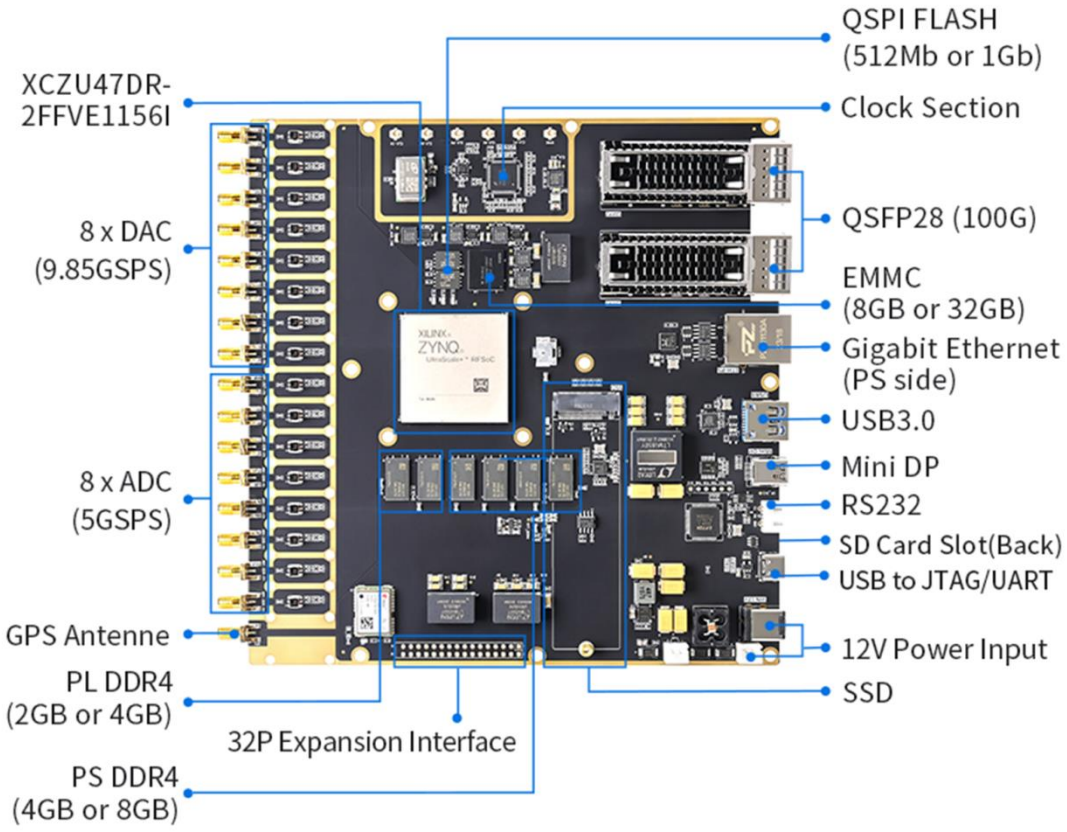
Part 1: P047_P047Pro Overview

1.1P047_P047Pro Introduction

The Puzhi Software Defined Radio (PZSDR) Series encompasses a diverse range of products. This document introduces the P047/P047Pro developed by Puzhi. The difference between the P047 and P047Pro lies in the different capacities of the DDR4, EMMC, and QSPI Flash used, which are elaborated in detail in Chapter 2. Both products adopt AMD's XCZU47DR-2FFVE1156I as the main controller, are equipped with 8-channel high-speed ADCs and 8-channel high-speed DACs, and integrate various hardware interfaces, offering rich resources and user-friendly operation. The product's internal resource structure is illustrated below.

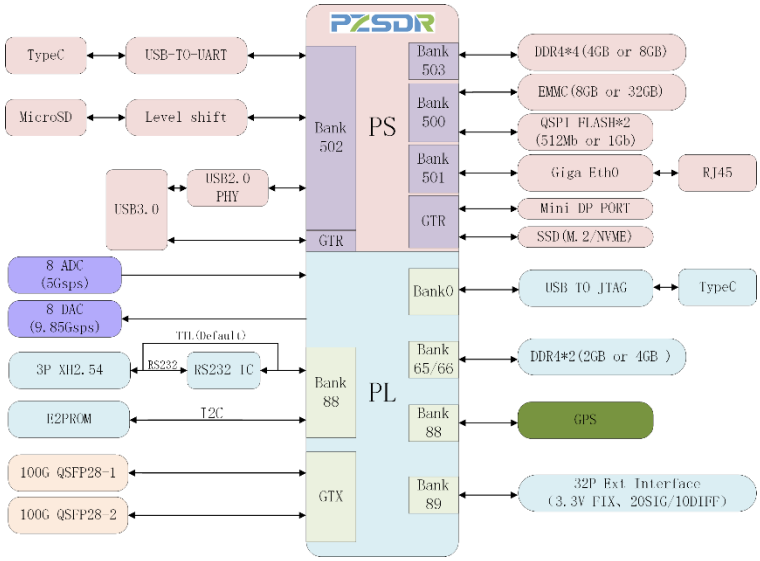
The PCB dimensions of the P047/P047Pro are 180mm (length)×175mm (width). The PCB reserves multiple mounting holes, facilitating direct integration into user equipment. Additionally, the product comes with an exquisite enclosure that serves a heat dissipation function, ensuring stable operation.

Designed to industrial-grade standards, the P047/P047Pro operates within a temperature range of -40℃ to 85℃, with all interfaces featuring ESD (Electrostatic Discharge) protection.



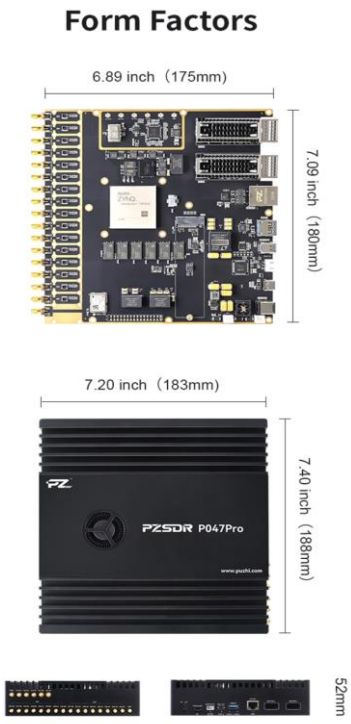
1.2 P047_P047Pro Block Diagram

The block diagram below outlines the product's on-board resources, and all functions included in the development board can be viewed in the table below.



1.3 P047_P047Pro Form Factors

The figure below illustrates the dimensions of the P047/P047Pro PCBA board and the customized shell respectively.**Note:** Enclosure logo customization is supported—users only need to provide the logo file to get an exclusive customized logo.



Part 2: Hardware User Manual

In this part, we will systematically introduce the various hardware functions of the P047/P047Pro board to help users get started quickly.

2.1 P047_P047Pro Framework Overview

The table below outlines the specifications of the P047/P047Pro board and the external resources of its design. The board adopts a single XCZU47DR-2FFVE1156I chip to design 8T/8R RF channels and multiple high-speed data transmission interfaces, fulfilling the full transmit-receive functionality of the entire link. As shown in the figure, we detail the differences in the DDR, EMMC, and QSPI FLASH resources between the P047 and P047Pro. For additional details, refer to the drawings provided by Puzhi.

SDR Module	P047	P047Pro
FPGA Chip	XCZU47DR-2FFVE1156I	
DDR4	PS Side 4GB、PLSide 2GB	PS Side 8GB、PLSide 4GB
QSPI FLASH	512Mb	1Gb
EMMC	8GB	32GB
Processor Core	ARM : 4 x Cortex-A53 1.333Ghz	RPU : 2 x Cortex-R5 533Mhz
Speed Grade	2	
Temperature Grade	Industrial Grade(-40°C~+85°C)	
Logic Cells	930k	
Look-Up Tables	425k	
DSP Slices	4272	
Block RAM	38Mb	
Boot Mode	JTAG/QSPI/SD/EMMC, selected via on-board DIP switch	
ADC Channels	8 Channels/Sample Rate 5Gsps	
DAC Channels	8 Channels/Sample Rate 9.85Gsps	
Number of Expansion IOs	HD: 20 (1.8/2.5/3.3V adjustable, default 3.3V)	
JTAG/UART	1 / 1	
TTL Serial Port/RS232	1	
SD Card Interface	1	
PS-side SSD Interface	1	
Gigabit Ethernet	PS Side 1 Gigabit Ethernet	
Mini DP Output	1	
USB3.0 Host/Device Port	1	
SSD Storage	1	
QSFP28 Interface	100G*2	
Form Factors	180mm x 175mm (7.09 inch x6.89 inch)	
Power Supply	12V/3A	

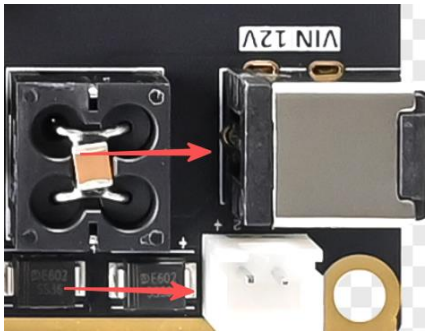
2.2 Power Supply

The P047/P047Pro supports two power supply options: XH2.54 and DC-007B interfaces, accommodating customer power needs across different usage scenarios.

XH2.54 Interface: For integration into user equipment, power is supplied via this interface with a 12V/3A specification.

DC-007B Interface: This interface connects to Puzhi's 12V/3A power adapter for power, featuring a plug-and-play design.

Note: The DC-007B and XH2.54 connectors are interconnected. For safety reasons, please connect only one power source to either of them at a time to prevent mutual interference between the two power supplies.



2.3 Clock Section

The P047/P047Pro board is designed with multiple clock channels to meet different functional requirements. For additional details, refer to the drawings provided by Puzhi.

(1) A 33.3333 MHz clock input is designed for the PS side, with the input pin named PS_REF_CLK and located at M25. This clock serves as the clock source for the ARM side.

(2) A 200 MHz clock is provided for the PL side, with the input pins IO_L13P_GC_66/IO_L13N_GC_66 mapped to locations AL9/AM9. This clock acts as the clock source for the PL side.

(3) Two clock channels are provided for the MGT section: 125 MHz and 156.25 MHz, with the following input pin mappings:

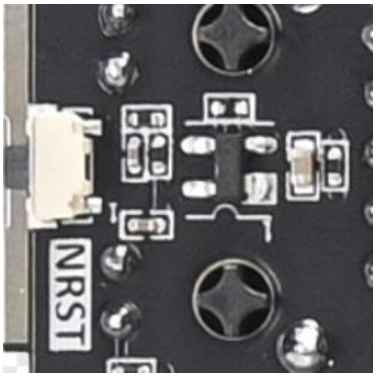
- 125 MHz clock: MGT_REF_CLK_P0_128/ MGT_REF_CLK_N0_128 (pin locations:M28/M29)
- 156.25 MHz clock: MGT_REF_CLK_P1_128/ MGT_REF_CLK_N1_128 (pin locations:K28/K29)

(4) Three clock channels (26MHz, 27MHz, 100MHz) are provided for the GTR section, allocated respectively to the USB 3.0, Mini DP, and SSD peripheral interfaces.

A dedicated clock chip is configured for the high-speed ADC/DAC circuits, outputting multiple clock channels to fulfill the synchronous operation requirements of single or multiple chips. In addition, the clock source of the dedicated clock chip can be selected via a DIP switch: either the on-board 19.2MHz OCXO or a higher-precision clock input through the IPEX connector. Here, the IPEX connector has been connected to the enclosure via an RF cable and converted to an SSMA interface marked as CLK-IN; users can locate the corresponding interface on the enclosure for connection.

2.4 Reset key

The P047/P047Pro board is equipped with an nGST (Global System Reset) reset button near the board edge, which functions as the system reset and is active-low. This pin connects to PS_POR_B (N24) on the PS side and IO_L2P_66 (AP6) on the PL side respectively.



2.5 Main Controller Boot Modes

The P047/P047Pro board supports four boot modes: JTAG, QSPI Flash, EMMC, and SD card. Boot mode selection is via board-edge DIP switches. Three DIP selector switches (M2/M1/M0) are shown below, with corresponding boot modes selected per the boot truth table.

BOOT MODE	M2	M1	M0
JTAG	0	0	0
QSPI FLASH	0	1	0
SD1 CARD	1	0	1
EMMC	1	1	0

2.6 DDR4 Introduction

The PS side of the P047/P047Pro board is designed with four industrial-grade DDR4 chips, and the PL side is equipped with two industrial-grade DDR4 chips.

For the P047: each PS-side DDR4 chip has a single-chip capacity of 1 GB, totaling 4 GB for four chips; each PL-side DDR4 chip has a single-chip capacity of 1 GB, totaling 2 GB for two chips.

For the P047Pro: each PS-side DDR4 chip has a single-chip capacity of 2 GB, totaling 8 GB for four chips; each PL-side DDR4 chip has a single-chip capacity of 2 GB, totaling 4 GB for two chips.

The pin assignment of the PS-side DDR4 can directly use the system-assigned configuration, and you may also refer to the example projects provided by Puzhi. The pin definitions of the PL-side DDR4 are detailed in the table below.

DDR4	Pin Name	Pin Position
PL_DDR4_D0	IO_L2P_65	AM15
PL_DDR4_D1	IO_L5N_65	AN17
PL_DDR4_D2	IO_L3N_65	AP15
PL_DDR4_D3	IO_L5P_65	AM17
PL_DDR4_D4	IO_L2N_65	AN15
PL_DDR4_D5	IO_L6P_65	AN18
PL_DDR4_D6	IO_L3P_65	AP16
PL_DDR4_D7	IO_L6N_65	AP17
PL_DDR4_DM0	IO_L1P_65	AM14
PL_DDR4_DQS_P0	IO_L4P_65	AL17
PL_DDR4_DQS_N0	IO_L4N_65	AM16
PL_DDR4_D8	IO_L8N_65	AK14
PL_DDR4_D9	IO_L9P_65	AK18
PL_DDR4_D10	IO_L11P_65	AJ16
PL_DDR4_D11	IO_L12P_65	AJ17
PL_DDR4_D12	IO_L11N_65	AJ15
PL_DDR4_D13	IO_L9N_65	AL18
PL_DDR4_D14	IO_L8P_65	AK15
PL_DDR4_D15	IO_L12N_65	AK16
PL_DDR4_DM1	IO_L7P_65	AH13
PL_DDR4_DQS_P1	IO_L10P_65	AH18
PL_DDR4_DQS_N1	IO_L10N_65	AJ18
PL_DDR4_D16	IO_L15P_65	AF14
PL_DDR4_D17	IO_L18N_65	AF17
PL_DDR4_D18	IO_L17N_65	AF16
PL_DDR4_D19	IO_L14P_65	AG17
PL_DDR4_D20	IO_L17P_65	AE16
PL_DDR4_D21	IO_L18P_65	AF18
PL_DDR4_D22	IO_L15N_65	AF13

PL_DDR4_D23	IO_L14N_65	AH17
PL_DDR4_DM2	IO_L13P_65	AG15
PL_DDR4_DQS_P2	IO_L16P_65	AG14
PL_DDR4_DQS_N2	IO_L16N_65	AH14
PL_DDR4_D24	IO_L21P_65	AD15
PL_DDR4_D25	IO_L23N_65	AD16
PL_DDR4_D26	IO_L20P_65	AE14
PL_DDR4_D27	IO_L24P_65	AD18
PL_DDR4_D28	IO_L20N_65	AE13
PL_DDR4_D29	IO_L23P_65	AC17
PL_DDR4_D30	IO_L21N_65	AE15
PL_DDR4_D31	IO_L24N_65	AE18
PL_DDR4_DM3	IO_L19P_65	AC13
PL_DDR4_DQS_P3	IO_L22P_65	AC16
PL_DDR4_DQS_N3	IO_L22N_65	AC15
PL_DDR4_A0	IO_L7P_66	AP13
PL_DDR4_A1	IO_L17P_66	AK10
PL_DDR4_A2	IO_L4N_66	AN4
PL_DDR4_A3	IO_L7N_66	AP12
PL_DDR4_A4	IO_L8N_66	AN12
PL_DDR4_A5	IO_L16P_66	AL12
PL_DDR4_A6	IO_L5N_66	AP2
PL_DDR4_A7	IO_L15N_66	AL13
PL_DDR4_A8	IO_L4P_66	AN5
PL_DDR4_A9	IO_L16N_66	AL11
PL_DDR4_A10	IO_T1U_66	AN9
PL_DDR4_A11	IO_L2N_66	AP5
PL_DDR4_A12	IO_L9N_66	AN7
PL_DDR4_A13	IO_L15P_66	AK13
PL_DDR4_A14	IO_L9P_66	AN8
PL_DDR4_A15	IO_L22N_66	AJ9
PL_DDR4_A16	IO_L10N_66	AM7
PL_DDR4_A17	IO_L18N_66	AK11
PL_DDR4_BA0	IO_L6P_66	AN2
PL_DDR4_BA1	IO_L8P_66	AN13
PL_DDR4_BG0	IO_L6N_66	AN1
PL_DDR4_nCS	IO_L3N_66	AM5
PL_DDR4_nACT	IO_L10P_66	AM8
PL_DDR4_ODT	IO_L1P_66	AP8
PL_DDR4_nRESET	IO_L5P_66	AP3
PL_DDR4_CLK_P	IO_L14P_66	AM12
PL_DDR4_CLK_N	IO_L14N_66	AM11

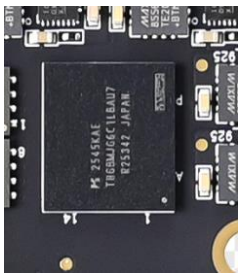
PL_DDR4_CKE	IO_L1N_66	AP7
PL_DDR4_PARITY	IO_L18P_66	AJ11
PL_DDR4_nALERT	IO_L22P_66	AJ10

2.7 EMMC Introduction

The P047 is equipped with an 8GB eMMC, and the P047Pro is equipped with a 32GB eMMC, which users can use to store boot files and user files.

The pin definitions are detailed in the table below.

EMMC	Pin Name	Pin Position
EMMC_D0	MIO13	G18
EMMC_D1	MIO14	A15
EMMC_D2	MIO15	D16
EMMC_D3	MIO16	G17
EMMC_D4	MIO17	E16
EMMC_D5	MIO18	F18
EMMC_D6	MIO19	C16
EMMC_D7	MIO20	B16
EMMC_CLK	MIO22	E17
EMMC_CMD	MIO21	F17
EMMC_nRST	MIO23	D17



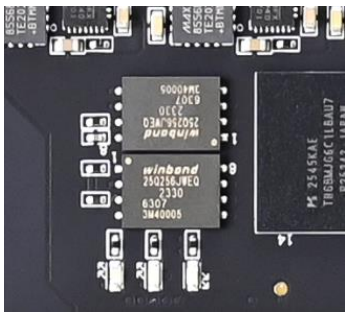
2.8 QSPI FLASH Introduction

The P047/P047Pro board is equipped with two channels of QSPI FLASH, with a total capacity of 512Mb for the P047 and 1Gb for the P047Pro. It can be used to store boot files and user files.

The pin definitions are detailed in the table below.

QSPI0 FLASH	Pin Name	Pin Position
QSPI0_DQ0	MIO4	G15
QSPI0_DQ1	MIO1	J18
QSPI0_DQ2	MIO2	J16
QSPI0_DQ3	MIO3	K16
QSPI0_CS	MIO5	H18
QSPI0_CLK	MIO0	J17

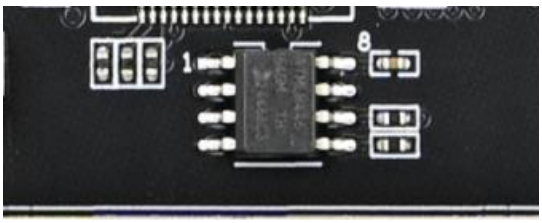
QSPI1 FLASH	Pin Name	Pin Position
QSPI1_DQ0	MIO8	E15
QSPI1_DQ1	MIO9	F15
QSPI1_DQ2	MIO10	C15
QSPI1_DQ3	MIO11	G16
QSPI1_CS	MIO7	K17
QSPI1_CLK	MIO12	B15



2.9 E2PROM Introduction

The P047/P047Pro board reserves one 64Kb E2PROM chip. The pin definitions are detailed in the table below.

E2PROM	Pin Name	Pin Position
E2PROM_I2C_SCL	IO_L12P_AD8P_88	B12
E2PROM_I2C_SDA	IO_L12N_AD8N_88	A12

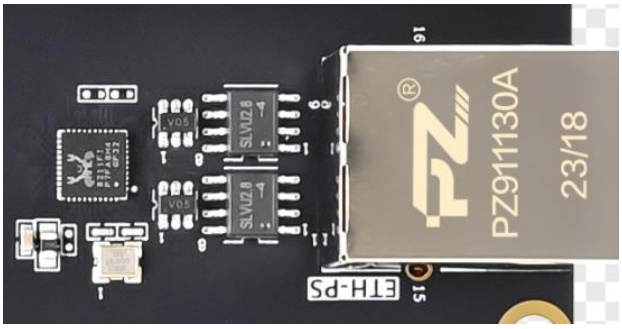


2.10 Gigabit Ethernet

The PS side of the P047/P047Pro board is designed with a Gigabit Ethernet chip, which interconnects with the ZYNQ chip via the RGMII interface. The corresponding connected pins are detailed in the table below. The PHY address is PHY_AD[2:0] = 001.

RGMII Signal	Pin Name	Pin Position
GPHY_GTX_CLK	MIO26_501	K19
GPHY_TXD0	MIO27_501	H19
GPHY_TXD1	MIO28_501	J19
GPHY_TXD2	MIO29_501	H21
GPHY_TXD3	MIO30_501	H20

GPHY_TX_EN	MIO31_501	G20
GPHY_RX_CLK	MIO32_501	F19
GPHY_RXD0	MIO33_501	G21
GPHY_RXD1	MIO34_501	D18
GPHY_RXD2	MIO35_501	F20
GPHY_RXD3	MIO36_501	C18
GPHY_RX_DV	MIO37_501	E19
GPHY_MDC	MIO76_502	E26
GPHY_MDIO	MIO77_502	D26

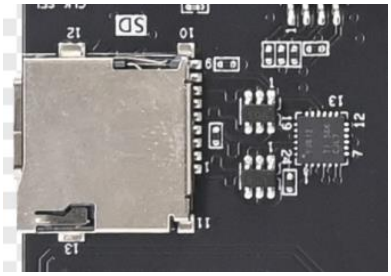


2.11 SD Card Slot Interface

The P047/P047Pro board features an SD card slot connected to BANK501 on the PS side. With BANK501 operating at 1.8 V and the SD card's data interface at 3.3 V, the TXS02612RTWR chip is used for level shifting.

SD card pin assignments are detailed below. For detailed circuit design, refer to the schematic.

SD card	Pin Name	Pin Position
SD_CLK	MIO51	B21
SD_CMD	MIO50	A22
SD_DATA0	MIO46	A20
SD_DATA1	MIO47	D21
SD_DATA2	MIO48	C21
SD_DATA3	MIO49	E21
SD_CD	MIO74	C26

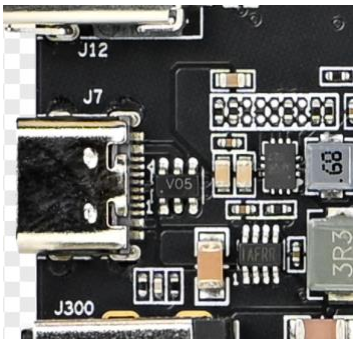


2.12 USB to JTAG/UART

The P047/P047Pro board features a USB-to-JTAG/UART interface: the JTAG segment connects to the main control chip's JTAG interface, while the UART segment connects to the chip's UART0 pins.

UART0 pin assignments are detailed below. For detailed circuit design, refer to the schematic.

UART0	Pin Name	Pin Position
UART0_TX	MIO43	A19
UART0_RX	MIO42	E20

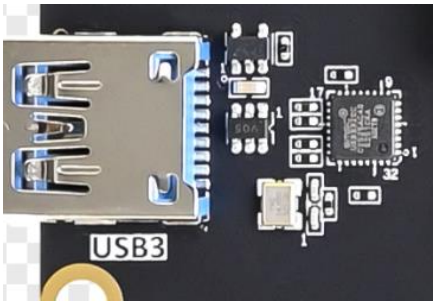


2.13 USB 3.0

The P047/P047Pro board features a USB 3.0 (Type-A) interface, configurable as either Host or Device mode.

The mapping between the USB PHY and main control chip is detailed in the table below. For additional details, refer to the board schematic.

USB signal pins	Pin Name	Pin Position
USBPHY_DATA0	MIO56	G23
USBPHY_DATA1	MIO57	F23
USBPHY_DATA2	MIO54	H23
USBPHY_DATA3	MIO59	D23
USBPHY_DATA4	MIO60	A23
USBPHY_DATA5	MIO61	E22
USBPHY_DATA6	MIO62	B23
USBPHY_DATA7	MIO63	C23
USBPHY_STP	MIO58	B22
USBPHY_NXT	MIO55	D22
USBPHY_DIR	MIO53	F22
USBPHY_CLKOUT	MIO52	G22
USBPHY_nRSET	MIO64	D24
GT2_USB3_SSTXP	PS_MGTRTXP2_505	U31
GT2_USB3_SSTXN	PS_MGTRTXN2_505	U32
GT2_USB3_SSRXP	PS_MGTRRXP2_505	V33
GT2_USB3_SSRXN	PS_MGTRRXN2_505	V34
CLK_FPGA_26M_P	MGT_505_TX_P2	T28
CLK_FPGA_26M_N	MGT_505_TX_N2	T29

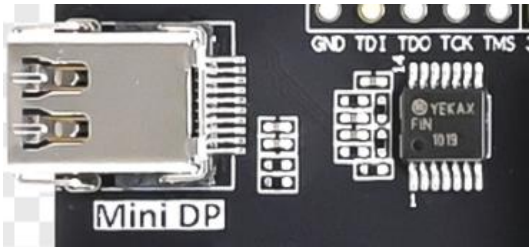


2.14 Mini DP

The P047/P047Pro board integrates a Mini DP output interface, whose interface signals connect to FPGA BANK88/BANK505. For details, refer to the schematic.

Mini DP interface pin assignments are listed below; refer to the development board schematic for detailed circuit implementation.

Mini DP	Pin Name	Pin Position
GT3_DP_LINE_P0	MGT_505_TX_P3	R30
GT3_DP_LINE_N0	MGT_505_TX_N3	R31
DP_HPD	IO_L5N_88	F13
DP_AUX_OUT	IO_L4P_88	H13
DP_OE	IO_L4N_88	G13
DP_AUX_IN	IO_L2N_88	H14
DP_CLK_P_27M	MGT_505_CLK_P3	P28
DP_CLK_N_27M	MGT_505_CLK_N3	P29



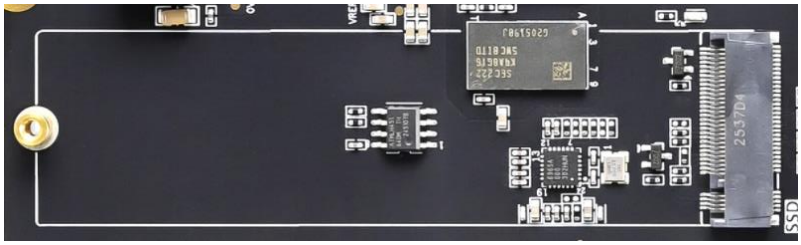
2.15 SSD interface

The P047/P047Pro board integrates an SSD interface (x2 mode) on its PS side, featuring an M.2 form factor and NVMe protocol compliance.

SSD interface pin locations are detailed in the table below; refer to the development board schematic for specific circuit implementation.

SSD interface	Pin Name	Pin Position
SSD_nRST	MIO70	B25
CLK_FPGA_100M_P	MGT_505_CLK_P0	Y29
CLK_FPGA_100M_N	MGT_505_CLK_N0	Y30

GT0_SSD_TX_P0	MGT_505_TX_P0	AA31
GT0_SSD_TX_N0	MGT_505_TX_N0	AA32
GT0_SSD_RX_P0	MGT_505_RX_P0	AB33
GT0_SSD_RX_N0	MGT_505_RX_N0	AB34
GT1_SSD_TX_P1	MGT_505_TX_P1	W31
GT1_SSD_TX_N1	MGT_505_TX_N1	W32
GT1_SSD_RX_P1	MGT_505_RX_P1	Y33
GT1_SSD_RX_N1	MGT_505_RX_N1	Y34



2.16 QSFP28 Interface

The P047/P047Pro board integrates two 100G QSFP28 interfaces, whose signals are connected to the MPSoC's BANK128/BANK129. For details, refer to the schematic.

The pin assignments for the QSFP28 interface are detailed in the table below. For the detailed circuit implementation, consult the development board schematic.

QSFP28	Pin Name	Pin Position
QSFP1_TX_P0	MGT-TX-P2-128	J30
QSFP1_TX_N0	MGT-TX-N2-128	J31
QSFP1_TX_P1	MGT-TX-P1-128	L30
QSFP1_TX_N1	MGT-TX-N1-128	L31
QSFP1_TX_P2	MGT-TX-P3-128	G30
QSFP1_TX_N2	MGT-TX-N3-128	G31
QSFP1_TX_P3	MGT-TX-P0-128	N30
QSFP1_TX_N3	MGT-TX-N0-128	N31
QSFP1_RX_P0	MGT-RX-P2-128	K33
QSFP1_RX_N0	MGT-RX-N2-128	K34
QSFP1_RX_P1	MGT-RX-P1-128	M33
QSFP1_RX_N1	MGT-RX-N1-128	M34
QSFP1_RX_P2	MGT-RX-P3-128	H33
QSFP1_RX_N2	MGT-RX-N3-128	H34
QSFP1_RX_P3	MGT-RX-P0-128	P33
QSFP1_RX_N3	MGT-RX-N0-128	P34
QSFP1_LPMODE	IO_L5P_88	F14
QSFP1_I2C_SCL	IO_L6P_88	G12
QSFP1_I2C_SDA	IO_L6N_88	F12

QSFP28	Pin Name	Pin Position
QSFP2_TX_P0	MGT-TX-P2-129	C30
QSFP2_TX_N0	MGT-TX-N2-129	C31
QSFP2_TX_P1	MGT-TX-P1-129	D28
QSFP2_TX_N1	MGT-TX-N1-129	D29
QSFP2_TX_P2	MGT-TX-P3-129	B28
QSFP2_TX_N2	MGT-TX-N3-129	B29
QSFP2_TX_P3	MGT-TX-P0-129	E30
QSFP2_TX_N3	MGT-TX-N0-129	E31
QSFP2_RX_P0	MGT-RX-P2-129	B33
QSFP2_RX_N0	MGT-RX-N2-129	B34
QSFP2_RX_P1	MGT-RX-P1-129	D33
QSFP2_RX_N1	MGT-RX-N1-129	D34
QSFP2_RX_P2	MGT-RX-P3-129	A31
QSFP2_RX_N2	MGT-RX-N3-129	A32
QSFP2_RX_P3	MGT-RX-P0-129	F33
QSFP2_RX_N3	MGT-RX-N0-129	F34
QSFP2_LPMODE	IO_L5P_88	F14
QSFP2_I2C_SCL	IO_L7P_88	E14
QSFP2_I2C_SDA	IO_L7N_88	D14

2.17 32P Expansion Interface

The P047/P047Pro board reserves a 2.54 mm-pitch 32-pin connector for extended signal connectivity, whose signals connect to FPGA BANK89 with a 3.3 V voltage level.

Signal-corresponding chip locations are listed in the table below; refer to the schematic section for detailed connection relationships.

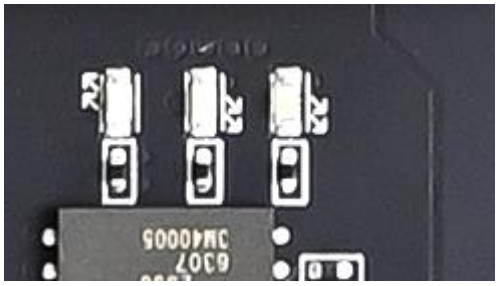
JM1 Signal	Pin Name	Pin	JM1 Signal	Pin Name	Pin

Sequence		Position	Sequence		Position
5	IO_L3P_89	A10	6	IO_L2P_89	C10
7	IO_L3N_89	A9	8	IO_L2N_89	B10
9	IO_L5P_HDGC_89	E11	10	IO_L1P_89	C11
11	IO_L5N_HDGC_89	D11	12	IO_L1N_89	B11
13	IO_L11P_89	J11	14	IO_L7P_89	F10
15	IO_L11N_89	H11	16	IO_L7N_89	F9
17	IO_L10P_89	K11	18	IO_L12P_89	K12
19	IO_L10N_89	K10	20	IO_L12N_89	J12
21	IO_L9P_89	H10	22	IO_L4P_89	D9
23	IO_L9N_89	H9	24	IO_L4N_89	C9

2.18 LED Indicators

The P047/P047Pro board integrates two LEDs configured in active-high mode: illuminated at high level and extinguished at low level. Refer to the development board schematic for detailed circuit implementation.

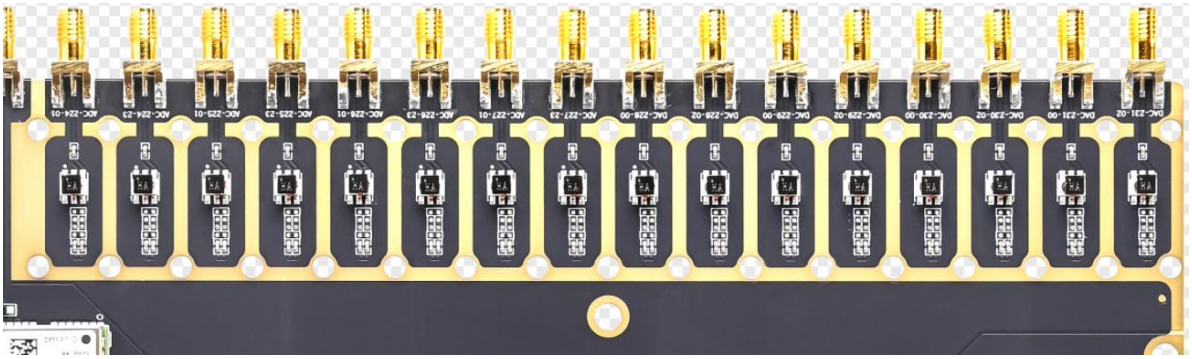
LED designator	Pin Name	Pin Position
LED1 (D17)	IO_L8P_88	E12
LED2 (D22)	IO_L8N_88	D12



2.19 High-Speed ADC/DAC

The P047/P047Pro board is equipped with 8 channels of high-speed ADCs and 8 channels of high-speed DACs. The ADC features a maximum sampling rate of up to 5 GSPS, and the DAC a maximum sampling rate of up to 9.85 GSPS. Both the ADCs and DACs offer 14-bit resolution; the DAC has a maximum output power of approximately 0 dBm, while the ADC supports a maximum input power of around 5 dBm. The synchronization error across all channels is no more than 3°, and multi-board synchronization is supported.

For more detailed information, refer to the development board schematic and example projects.



2.20 GPS Module

The P047/P047Pro board integrates a GPS module that supports both GPS and BeiDou positioning. The module is configurable and its data readable via the UART interface; moreover, it provides a PPS signal.

GPS module pin mappings are listed in the table below. For detailed specifications, refer to the provided schematic.

GPS Module	Pin Name	Pin Position
GPS_UART_TXD	IO_L9P_88	D13
GPS_UART_RXD	IO_L3P_88	J14
GPS_nRESET	IO_L1P_88	K15
GPS_PPS	IO_L1N_88	K14